AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-26. (Canceled).

27. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including a first and second region separated by an isolation element;

a first transistor formed on the first region of the substrate and including a first insulation film and a first gate electrode arranged along a first direction; and

a second transistor formed on the second region of the substrate and including a second insulation film and a second gate electrode arranged along the first direction,

wherein a side wall of the first gate electrode is directly physically and without the presence of additional layers therebetween connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction.

28. (Previously Presented) A device according to claim 33, wherein a side of the side insulator film is on a surface of said semiconductor substrate.

29. (Canceled).

30. (Previously Presented) A device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.

31. (Previously Presented) A device according to claim 33, wherein said first insulation film is thinner than said second insulation film, said first transistor forms a logic circuit, and said second transistor forms a memory cell.

32. (Previously Presented) A device according to claim 33, wherein top surfaces of said first and second gate electrodes are coplanar.

33. (Previously Presented) A device according to claim 34, wherein said second transistor further comprises a polysilicon layer formed on the second insulation film formed on the substrate, a side insulator film is formed on a side of the second insulation film and a side wall of the polysilicon layer, said second gate electrode is formed on the polysilicon layer, and the side wall of said first gate electrode is connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film.

34. (Previously Presented) A device according to claim 27, wherein the side wall of the first gate electrode is directly connected to the side wall of the second gate electrode.